DETAILED ACTION

1. Claim(s) 1-7, 9, 14-27, 29, 34-40 and 44 are presented for examination based on the amendment filed 04/25/2011.
2. Claim(s) 8, 10-13, 28, 30-33, 41-43, 45-47 are cancelled.
3. Claim(s) 1, 21 and 44 are amended.
4. In view of the papers filed 11/8/2010, it has been found that this nonprovisional application, as filed, through error and without deceptive intent, improperly set forth the inventorship, and accordingly, this application has been corrected in compliance with 37 CFR 1.48(a). The inventorship of this application has been changed by adding inventor Eric J. Strang.

   The application will be forwarded to the Office of Initial Patent Examination (OIPE) for issuance of a corrected filing receipt, and correction of Office records to reflect the inventorship as corrected.
5. Rejection(s) under 35 USC 112 for claim(s) 1-7, 9-11, 14-27, 29-31,34-10 and 44-46 is withdrawn in view of their amendment and arguments presented by the applicant on Remarks Pgs.13-17 which explicitly map each limitation.
6. Rejection(s) under 35 USC 102/103 for claim(s) 1-7, 9-11, 14-27, 29-31,34-10 and 44-46 are withdrawn in view of their amendment and arguments on Remarks Pgs.17-23 which are found to be persuasive.
7. Terminal Disclaimer filed 05/23/2008 against 10/673,583 and 10/673,501 is noted and approved on 06/04/2008.
8. Claim(s) 1-7, 9, 14-27, 29, 34-40 and 44 are allowed.

Allowable Subject Matter

9. The following is an **examiner's statement of reasons for allowance:** claim(s) 1-7, 9, 14-27, 29, 34-40 and 44 are considered allowable since when reading the claims in light of the specification, none of the references of record alone or in combination disclose or suggest the combination of limitations specified in the independent claims, specifically "*1) spatially resolved model of a physical geometry of the semiconductor processing tool 2) grid set addressing the semiconductor processing tool or a geometry of the semiconductor processing tool* (as defined in specification: [0076])... *using code parallelization techniques on multiple simulation modules in the device manufacturing fab, and re-using known simulation solutions as initial conditions for the first principles simulation* (as defined in specification: [0049][0050]) *wherein re-using known simulation solutions comprises searching in the fab-level library for a closest fitting solution which if used for the initial condition would reduce the number of iterations required by the simulation module"* (as defined in specification: [0076]), as disclosed in independent claims 1, 21 and 44 of the instant application.

Prior Art of Record

10. The Prior art of reference **Jain** (NPL) discloses teaches distributed simulation spanned over multiple simulation modules however does not teach grid set addressing of semiconductor tool or its geometry and fails to reuse the known simulation results to solve the computer-encoded differential equations of the first principles simulation physical model for the spatially resolved model concurrently

with the actual process being performed and in a time frame shorter in time than the actual process being performed.

11. The Prior art of reference **Tan** (US Patent No. US 6263255 B1) discloses process model and feed-forward and feed-back correction, however is also silent on grid set addressing of semiconductor tool or its geometry and fails to reuse the known simulation results.

12. The Prior art of Reference **Sonderman** (US Patent 6802045 B1) describes producing process parameters in a simulation environment for use in a manufacturing environment in semiconductor wafer processing (Sonderman: col. 4, 1.47 - col. 5, 1. 10), which does not teach the claimed invention which requires solve the computer-encoded differential equations of the first principles simulation physical model for the spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed.

Prior Art based on Updated Search

13. The Prior art **Su** et al (Reference AO on PTO 1449 dated 4/24/2011 on application 10/673138) teaches virtual fab (VF) as simulation tools to run in parallel With or before the actual fab for fast process, product, and operational developments, however it also does not teach grid set addressing of semiconductor tool or its geometry and fails to reuse the known simulation results to solve the computer-encoded differential equations of the first principles simulation physical model for the

spatially resolved model concurrently with the actual process being performed and in a time frame shorter in time than the actual process being performed.

14. The Prior art **Allen** (US Patent No. US 6763277 B1) a simulation environment capable of simulating at least one process operation performed on a semiconductor wafer and generating simulation data; a process scheduling model in communication with the simulation environment, the process scheduling model capable of performing a process scheduling function based upon at least one of the simulation data and a metrology data, to control the process operation; and a process control in communication with the process scheduling model, the process control capable of performing a line balancing function to control a processing of at least one semiconductor wafer based upon the process scheduling function. Allen does not teach simulation in a shorter time period than actual process.

15. The Prior art **Patel** (US PGPUB 20050010319) teaches canonical model simulating the actual process, however it is used for validation and verification ([0033][0040]-[0043]).

16. The Prior art **Enda** (US Patent No. US 6304834) teaches using grid based approach for semiconductor simulation and even modifies the solution (re-using it) (Enda: Fig.8B), however fails to teach that the solution is found in shorter time frame than the actual process (Enda: Fig.11).

17. The Prior art **Riley** et al (US PGPUB 20020107604) teaches rapid thermal processing (RTP) model(ing) in conjunction with actual semiconductor processing with feed back (Fig.1), however it appears that it also does not teach performing

simulation concurrently with the actual process being performed and *in a time frame shorter in time than the actual process being performed.*

18. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AKASH SAXENA whose telephone number is (571)272-8351. The examiner can normally be reached on 8:00- 6:00 PM Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit 2128

/Akash Saxena/
Examiner, Art Unit 2128